REMARKS

Claims 1 and 5-16 are pending in the application. Claims 3, 4 and 17-23 have been canceled in previous amendments. Claims 1, 5 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao et al., Satou et al. and Byers et al. Claims 6-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao, Byers and Satou as applied to claim 1, and further in view of Radogna et al. Claims 14 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao, Byers and Satou as applied to claims 1 and 15, and further in view of Muller et al. Reconsideration and reexamination of the application in view of the following remarks is respectfully requested.

The present invention is directed to enabling data communication between a storage area network and another network implementing a different protocol. Two microsequencer systems are employed to perform translations between the two different protocols *in both directions*. For example, *one microsequencer system* may be employed to perform a *translation from a first to a second protocol, and the other microsequencer system* may perform a *translation from the second to the first protocol.*

Claims 1, 5 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao, Satou and Byers. This rejection is respectfully traversed.

Claim 1 recites (1) a first microsequencer system configured to *translate* said second input data (in a *second network protocol*) into corresponding data expressed in said *first network protocol*, and (2) a second microsequencer system configured to *translate* said first input data (in a *first network protocol*) into corresponding data expressed in said *second network protocol.*

Similarly, claim 15 recites first and second processing elements in communication with said first and second input ports, one of the processing elements for *translating* input data from said *first network protocol* to said *second network protocol*, and the other for *translating* input data from said *second network protocol* to said *first network protocol.*

Yao, Satou and Byers all fail to disclose, teach or suggest a first microsequencer (processing element) for translating input data from a first network protocol to a second network protocol, and a second microsequencer (processing element) for translating input data from a second network protocol to a first network protocol as recited in claims 1 and 15.

Byers discloses two microsequencer bus controllers (uSBCs) as shown in FIGs. 25A (see reference characters 5002 and 5004) or FIG. 45 (see reference characters 3220 and 3222). However, both of these uSBCs execute *the same instruction stream* from a control store *in parallel* (see col. 30 lines 59-62 or col 57 lines 1-14), with one uSBC acting as a master and the other uSBC acting as a slave. Byers contains no disclosure at all related to first and second microsequencers that translate input data from a first network protocol to a second protocol, and vice versa, as recited in claims 1 and 15.

Yao does not disclose any microsequencers at all. Yao only discloses a number of *translation or routing tables* needed for address translation between network devices utilizing different protocols. For example, Yao discloses a translation table 205 in FIG. 9 which is used by addressing software when transmitting a frame from a Fibre Channel host to an iSCSI device (paragraph [0050]), and when transmitting a frame from an iSCSI host to a Fibre Channel device (paragraph [0052]). Other *translation or routing tables* for performing different translations are shown in FIGs. 11, 12, 13, 17 and 18 of Yao. However, the different tables disclosed in Yao are merely unrelated collections of associated addresses operated upon by addressing software. In other words, Yao takes a brute force approach of simply using a different translation table to perform different protocol translations. Tables and microsequencers (processing elements) are very different entities that cannot be equated or analogized, and it would not have been obvious at all from the simple translation tables disclosed Yao to implement multiple microsequencers (processing elements) as recited in claims 1 and 15.

Satou discloses only a single microsequencer. Satou is directed to a data processor that processes string operation instructions, but does not translate between two different network protocols in both directions, as recited in claims 1 and 15.

Because neither Yao, Satou nor Byers, alone or in combination, discloses, teaches or suggests all of the limitations of claims 1 and 15, it is respectfully submitted that the rejection of claims 1 and 15 under 35 U.S.C. §103(a) as being unpatentable over Yao and Satou has been traversed. In addition, because claim 5 depends from claim 1, the rejection of claim 5 is traversed for the same reasons provided above with respect to claim 1.

Claims 6-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao, Byers and Satou as applied to claim 1, and further in view of Radogna. This rejection is respectfully traversed.

Claims 6-13 depend from claim 1. As explained above, neither Yao, Satou, nor Byers, alone or in combination, discloses, teaches or suggests all of the limitations of claim 1. Furthermore, Radogna fails to make up for the deficiencies of Yao, Satou and Byers.

Radogna fails to disclose, teach or suggest first and second microsequencers that translate input data from a first network protocol to a second protocol, and vice versa, as recited in amended claim 1. Radogna discloses only a *single* microsequencer 100 (see FIG. 3 of Radogna) for performing header translation for frames being moved from an input FIFO to an output FIFO. Because Radogna is a unidirectional system, it understandably fails to disclose, teach or suggest a second microsequencer for header translation of frames being moved in the opposite direction.

Therefore, even if one skilled in the art would have been motivated to combine Yao, Satou, Byers and Radogna, none of those references discloses, teaches or suggests first and second microsequencer systems for performing protocol conversion in both directions, as recited in claim 1.

Because neither Yao, Satou, Byers nor Radogna, alone or in combination, discloses, teaches or suggests all of the limitations of claim 1, and because claims 6-13 depend from claim 1, it is respectfully submitted that the rejection of claims 6-13 under 35 U.S.C. §103(a) as being unpatentable over Yao, Satou, Byers and Radogna has been overcome.

Claims 14 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yao, Byers and Satou as applied to claims 1 and 15, and further in view of Muller. Claim 14 depends from claim 1, and claim 16 depends from claim 15.

As described above, neither Yao, Byers nor Satou, alone or in combination, discloses, teaches or suggests first and second microsequencer systems/processing elements for performing protocol conversion in both directions, as recited in amended claims 1 and 15.

Furthermore, Muller fails to make up for the deficiencies of Yao Byers and Satou. Muller is directed to a network interface for receiving a packet from a network and transferring it to a host computer system. The header of a packet may be parsed by a *single* microsequencer located in a parser module 106 (see FIG. 1A and col. 24 lines 12-67). Muller does not translate between two different network protocols in both directions, and therefore fails to disclose, teach or suggest a second microsequencer for parsing headers in packets in a different protocol.

Therefore, even if one skilled in the art would have been motivated to combine Yao, Byers, Satou and Muller, none of those references discloses, teaches or suggests first and second processing elements for performing protocol conversion in both directions, as recited in claims 1 and 15.

Because neither Yao, Byers, Satou nor Muller, alone or in combination, discloses, teaches or suggests all of the limitations of claims 1 and 15, and because claim 14 depends from claim 1 and claim 16 depends from claim 15, it is respectfully submitted that the rejection of claims 14 and 16 under 35 U.S.C. §103(a) as being unpatentable over Yao, Byers, Satou and Muller has been overcome.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If, for any reason, the Examiner finds the application other than in condition for allowance, Applicants request that the Examiner contact the undersigned attorney at the Los Angeles telephone number (213) 892-5752 to discuss any steps necessary to place the application in condition for allowance.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. 491442004500.

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Respectfully submitted,

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